REMARKS

Claims 1-16, 24, 26, 28 and 30-34 are pending in the present application.

Claim Rejections-35 U.S.C. 103

Claims 1, 5, 9, 13, 31 and 33 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Imai reference (U.S. Patent No. 6,344,675), in view of the Gallagher et al. reference (U.S. Patent No. 4,968,644). This rejection is respectfully traversed for the following reasons.

The field effect transistor of claim 1 features in combination "wherein a contact specific resistance between the metallic silicide layers and the impurity layers is less than 1 X 10^{-7} Ω - cm^{-2}, and wherein the semiconductor layer has a thickness of 20 nm". Applicants respectfully submit that the prior art as relied upon by the Examiner does not make obvious these features.

The Examiner has relied upon the Imai reference as in the previous Office Action dated August 8, 2005. The Examiner has however acknowledged that the Imai reference fails to teach a contact specific resistance between the metallic silicide layers and the impurity layers that is less than 1 X 10^{-7} Ω - cm^{-2}. In an effort to overcome this acknowledged deficiency of the primarily relied upon prior art, the Examiner has alleged that the Gallagher et al. reference discloses the above noted features regarding contact specific resistance between metallic silicide layers and impurity layers in column 10, lines 15-28.

The Examiner has characterized source 80 and drain 90 as shown in Fig. 5 of the Gallagher et al. reference as the pair of impurity layers of claim 1. As described beginning in column 10, line 15 of the Gallagher et al. reference, in a further embodiment not essential to the disclosed invention, regions of metal silicide (not shown) are fabricated on the sources and drains (80 and 90), prior to forming diffusion barriers (tungsten barrier 130 and 140 shown in Fig. 6).

Applicants respectfully submit that these unillustrated regions of metallic silicide as described in column 10 of the Gallagher et al. reference cannot be interpreted as the metallic silicide layers of claim 1. Particularly, the metallic silicide layers of claim 1 are featured as respectively formed **in** the source and drain regions. In contrast, the regions of metallic silicide of the Gallagher et al. reference as relied upon are formed **on** the source and drain regions. Moreover, the regions of metallic silicide of the Gallagher et al. reference do not have bottom surfaces that extend to bottom surfaces of a semiconductor layer, as would be necessary to meet the further features of claim 1. Since the unillustrated regions of metallic silicide of the Gallagher et al. reference cannot be interpreted as the metallic silicide layers of claim 1, the Gallagher et al. reference does not overcome the acknowledged deficiencies of the primarily relied upon Imai reference.

With further regard to this rejection, the Imai reference is directed to an SOI-MOS field effect transistor including SOI layer 3 on insulating layer 2, as shown in Fig. 12 for example. In contrast, the MOSFET as described with respect to Figs. 1-7 of the

Gallagher et al. reference includes a layer of doped semiconductor material 20 serving as a surface active layer of substrate 10 of semiconductor material. The Gallagher et al. reference is not directed to an SOI-MOS field effect transistor. It is thus unclear how one of ordinary skill would be led to modify the Imai and Gallagher et al. references as taken together to provide a semiconductor layer having a thickness of 20 nm, as would be necessary to meet the further features of claim 1. Applicants therefore respectfully submit that the field effect transistor of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 1 is improper for at least these reasons.

Applicants further respectfully submit that respective independent claims 5, 9 and 13 would not have been obvious in view of the prior art as relied upon by the Examiner for at least somewhat similar reasons as set forth above. The metallic silicide layers of claim 5 are featured as in the source and drain regions. The source and drain regions of claim 9 are respectively featured as including first and second metallic silicide layers. The source and drain regions of claim 13 are respectively featured as including first and second metallic silicide layers. In contrast, the Gallagher et al. reference as secondarily relied upon describes unillustrated regions of metallic silicide on sources and drains.

Additionally, the metallic silicide layers of claim 5 are further featured as having a thickness which is equal to or more than 80% thickness of from an upper surface of the metallic silicide layers to a bottom surface of the semiconductor layer. In claim 9, the

first and second metallic silicide layers are respectively featured as reaching the insulating layer through the semiconductor layer. In claim 13, the first and second metallic silicide layers are respectively featured as having a thickness which is equal to or more than 80% a thickness from an upper surface of the metallic silicide layers to a bottom surface of the semiconductor layer. The Gallagher et al. reference as relied upon does not disclose these respective features. Applicants therefore respectfully submit that the field effect transistors of respective claims 5, 9 and 13 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 5, 9, 13, 31 and 33 is improper for at least these reasons.

Claims 2, 6, 10 and 14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Imai reference in view of the Gallagher et al. reference, in further view of Applicant's admitted prior art. Applicants respectfully submit that Applicants' admitted prior art as relied upon by the Examiner does not overcome the above noted deficiencies of the primarily relied upon prior art. Applicants therefore respectfully submit that claims 2, 6, 10 and 14 would not have been obvious in view of the prior art as relied upon by the Examiner for at least these additional reasons.

Allowable Subject Matter

Applicants respectfully note the Examiner's acknowledgement that claims 3, 4, 7, 8, 11, 12, 15, 16, 24, 26, 28, 30, 32 and 34 are allowed.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

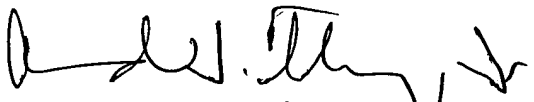
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicants hereby petition for an extension of two (2) months to September 18, 2006, for the period in which to file a response to the outstanding Office Action. The required fee of $450.00 is attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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